EE222 Midterm Examination

February 5, 2019

Name_____ Student ID_____

1. (10 points) In VLSI development estimation of required design effort in terms of engineer-months (EMs) is important. A handy empirical formula is shown below:

   EM = $(1 + D)^{-yr}$ (A + $B.k^H$), where k represents the number of equivalent transistors in the design expressed as

   k = UNQ + C. RPT + E. PLA + F. $\sqrt{RAM}$ + G. $\sqrt{ROM}$

in units of thousands (which means for 1M transistors in random access memory, RAM=1000) and A, B, C, D, E, F, G, and H are parameters that depend on the designers' experience and CAD tool support for the particular VLSI development .

Three years prior to the current project (thus yr = 3), the fitting parameters were

A=0, B=12, C= 0.15, D= 0.15, E = 0.1, F = 0.2, G = 0.1, and H=1.2.

For a GPU development the estimated number of transistors are Random Access Memory- 3.6M transistors, Read Only Memory- 0.1M transistors, PLA transistors-0.4M transistors, Unique transistors- 0.1M transistors, Repeated transistors- 0.4M transistors

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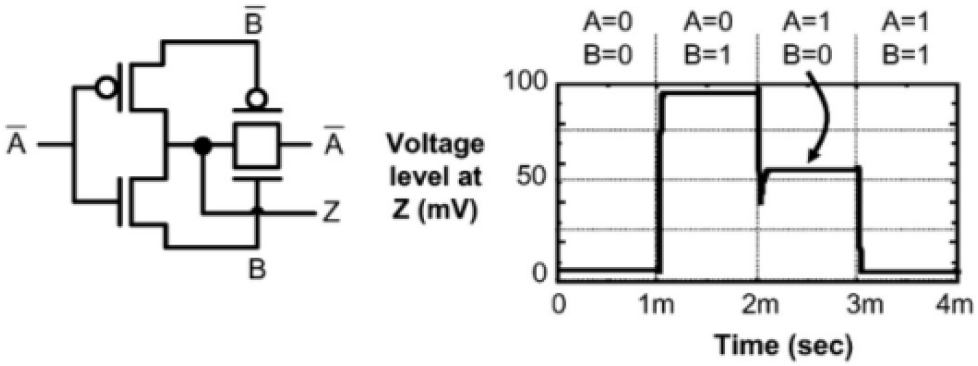
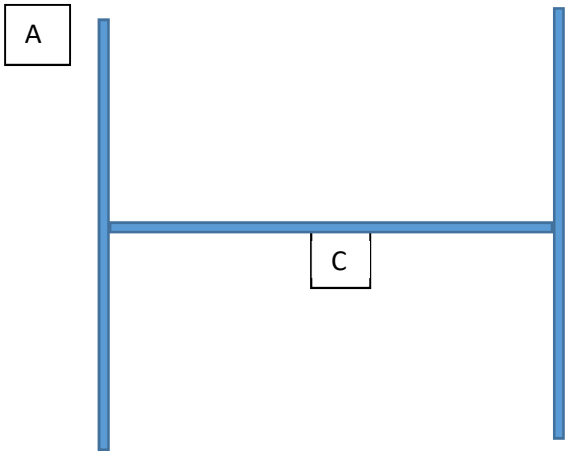
For the 20-engineer design team, estimate the numbers of months required for developing the GPU chip described above.

2. (20 points) For low power operation of CMOS circuits, **describe the design principles** in terms of speed requirement (delay specification), power supply voltages V_{DD} (multiple values), voltage swings ΔV at output nodes, switched capacitances C_{sw}(= product of switching frequency and capacitances), and MOS transistors' threshold voltages V_{th} (multiple values). For total power consumption, please include dynamic (switching) power, leakage power, and short circuit power.

3. (20 points) Explain why the output voltage Z of an XOR gate is only about 50 mV for the time period of 2mS <t< 3mS. What would cause this malfunction in this circuit?



4. (20 points) Let us consider an H-tree metal interconnect configuration of a uniform width 1 µm that distributes a clock signal from point C to four regions. Its horizontal length is 1000 µm and its vertical lengths are also 1000 µm. Assuming that the line resistance is 0.05 Ω/square, and the effective line capacitance including the fringing field effect is 0.05 fF/ μm^2, **find the Elmore delay from the center point C to the top left corner A.** For simple analysis use a distributed L-type RC model for every 250 µm.



5. (30 points) A super buffer can be used to drive a large load capacitance C_{load} instead of abruptly enlarging the driving gate's transistor sizes. When the total input gate capacitance of an intrinsic inverter is C_g =0.083fF and C_{load}= 1.828 pF, **find the minimum delay achievable in picoseconds**. It is known that the ring oscillator frequency is 200 GHz when 15 intrinsic inverters are cascaded. (Hint: The intrinsic inverter delay τ_o can be found from the oscillation frequency. Also C_{load}/C_g = e^{10} for e= 2.718.)

(for continuation)